CLAIMS

What is claimed is:

1. An apparatus for determining a processing speed of an integrated circuit, the apparatus comprising:

a first flip flop having an input port capable of receiving an input signal, an output port capable of providing a flip flop output signal and a timing port capable of receiving an incoming clock signal;

a delay circuit operably coupled to the output port of the first flip flop such that the delay circuit is capable of receiving the flip flop output signal and generating a delay timing signal;

at least one clock speed adjusting circuit operably coupled to the delay circuit;

a multiplexer operably coupled to the at least one clock speed adjusting circuit and the delay circuit, wherein the multiplexer has a select delay input port capable of receiving a select delay signal such that the multiplexer generates a multiplexer output signal corresponding to at least one of: an output signal generated by the at least one clock speed adjusting circuit and the delay timing signal; and

a second flip flop having an input port capable of receiving the multiplexer output signal, an output port capable of providing a timing output signal and a timing port capable of receiving the incoming clock signal.

2. The apparatus of claim 1 further comprising:

a pseudo-random input generator operably coupled to the first flip flop, such that the pseudo-random input generator generates the input signal.

3. The apparatus of claim 2 further comprising:

a sequencer operably coupled to the multiplexer, such that the sequencer generates the select delay signal.

4. The apparatus of claim 1 further comprising:

a logic gate coupled to the second flip flop such that the logic gate receives the timing output signal and generates a timing indicator signal.

5. The apparatus of claim 1 further comprising:

a pseudo-random input generator operably coupled to the first flip flop, such that the pseudo-random input generator generates the input signal;

a sequencer operably coupled to the multiplexer, such that the sequencer generates the select delay signal;

a logic gate coupled to the second flip flop such that the logic gate receives the timing output signal and generates a timing indicator signal; and

a register coupled to receive the select delay signal and the timing indication signal.

6. The apparatus of claim 1 wherein the delay circuit includes at least one delay buffer and a plurality of gates.

7. The apparatus of claim 1 wherein the at least one clock speed adjusting circuit includes at least on delay buffer and a plurality gates.

8. An apparatus for determining a processing speed of an integrated circuit, the apparatus comprising:

a first flip flop having an input port capable of receiving an input signal, an output port capable of providing a flip flop output signal and a timing port capable of receiving an incoming clock signal;

a first delay module coupled to the first flip flop such that the first delay module receives the flip flop output signal, the first delay module operably coupled to receive the incoming clock signal and operably coupled to receive a select delay signal; and

a second delay module coupled to the first delay module such that the second delay module receives an interim timing output signal from the first delay module, the second delay module operably coupled to receive the incoming clock signal, such that the second delay module generates a timing output signal.

9. The apparatus of claim 8 further comprising:

a pseudo-random input generator operably coupled to the first flip flop, such that the pseudo-random input generator generates the input signal.

10. The apparatus of claim 9 further comprising:

a sequencer operably coupled to the multiplexer, such that the sequencer generates the select delay signal.

11. The apparatus of claim 8 further comprising:

a logic gate coupled to the second flip flop such that the logic gate receives the timing output signal and generates a timing indicator signal.

12. The apparatus of claim 8 further comprising:

a pseudo-random input generator operably coupled to the first flip flop, such that the pseudo-random input generator generates the input signal;

a sequencer operably coupled to the multiplexer, such that the sequencer generates the select delay signal;

a logic gate coupled to the second flip flop such that the logic gate receives the timing output signal and generates a timing indicator signal; and

a register coupled to receive the select delay signal and the timing indication signal.

13. The apparatus of claim 12 further comprising:

a plurality of control timing flip flops operably coupled to the pseudo-random input generator and coupled to receive the incoming clock signal such that the plurality of control timing flip flops generate a control timing signal, wherein the control timing signal is provided to the logic gate for comparison with the timing indicator signal; and

a logic gate flip flop coupled between the logic gate and the register wherein the logic gate flip flop is operably coupled to receive the incoming clock signal and the a timing indicator signal and generate a timing result signal provided to the register.

14. The apparatus of claim 8 wherein the first delay module includes:

a first delay circuit operably coupled to the output port of the first flip flop such that the first delay circuit is capable of receiving the flip flop output signal and generating a first delay timing signal;

at least one clock speed adjusting circuit operably coupled to the first delay circuit;

a first multiplexer operably coupled to the at least one clock speed adjusting circuit and the delay circuit, wherein the first multiplexer has a select delay input port capable of receiving the select delay signal such that the first multiplexer generates a first multiplexer output signal corresponding to at least one of: an output signal generated by the at least one clock speed adjusting circuit and the delay timing signal; and

a second flip flop having an input port capable of receiving the first multiplexer output signal, an output port capable of providing the interim timing output signal and a timing port capable of receiving the incoming clock signal.

15. The apparatus of claim 8 wherein the second delay module includes:

a second delay circuit operably coupled to the output port of the second flip flop such that the second delay circuit is capable of receiving the flip flop output signal and generating a second delay timing signal;

at least one clock speed adjusting circuit operably coupled to the second delay circuit;

a second multiplexer operably coupled to the at least one clock speed adjusting circuit and the delay circuit, wherein the second multiplexer has a select delay input port capable of receiving the select delay signal such that the second multiplexer generates a second multiplexer output signal corresponding to an output signal

generated by at least one of: the at least one clock speed adjusting circuit and the delay timing signal; and

a third flip flop having an input port capable of receiving the second multiplexer output signal, an output port capable of providing the timing output signal and a timing port capable of receiving the incoming clock signal.

16. A method for determining a processing speed of an integrated circuit comprising:

(a) receiving an input signal and an incoming timing signal in a first flip flop to generate a first flip flop output signal;

(b) providing the first flip flop output signal to a delay circuit to generate a delay timing signal;

(c) providing the delay timing signal to at least one clock speed adjusting circuit to generate a plurality of timing adjusted signals;

(d) providing the plurality of timing adjusted signals to a multiplexer;

(e) receiving a select delay signal in the multiplexer such that the multiplexer selects one of the plurality of timing adjusted signals to generate a multiplexer output signal;

(f) providing the multiplexer output signal to a second flip flop;

(g) receiving the incoming timing signal in the second flip flop to generate an output timing signal; and

(h) comparing the output timing signal with a control timing signal.

17. The method of claim 16 further comprising:

(i) receiving the input signal from a pseudo-random generator;

(j) receiving the select delay signal from a sequencer; and

(k) generating a timing result signal based on the comparison of the output timing signal and the control timing signal.

18. The method of claim 17 further comprising:

(l) providing the timing result signal to a register.

19. The method of claim 18 further comprising:

(m) repeating (a) through (l) to generating a plurality of timing result signals; and

(n) calculating the processing speed of the integrated circuit based on the plurality of timing result signals.

20. An apparatus for determining a processing speed of an integrated circuit, the apparatus comprising:

a first flip flop having an input port capable of receiving an input signal, an output port capable of providing a flip flop output signal and a timing port capable of receiving an incoming clock signal;

a first delay module coupled to the first flip flop such that the first delay module receives the flip flop output signal, the first delay module operably coupled to receive the incoming clock signal and operably coupled to receive a select delay signal, wherein the first delay module includes:

a first delay circuit operably coupled to the output port of the first flip flop such that the first delay circuit is capable of receiving the flip flop output signal and generating a first delay timing signal;

at least one clock speed adjusting circuit operably coupled to the first delay circuit;

a first multiplexer operably coupled to the at least one clock speed adjusting circuit and the delay circuit, wherein the first multiplexer has a select delay input port capable of receiving the select delay signal such that the first multiplexer generates a first multiplexer output signal corresponding to at least one of: an output signal generated by the at least one clock speed adjusting circuit and the delay timing signal; and

a second flip flop having an input port capable of receiving the first multiplexer output signal, an output port capable of providing the interim timing

output signal and a timing port capable of receiving the incoming clock signal; and

a second delay module coupled to the first delay module such that the second delay module receives an interim timing output signal from the first delay module, the second delay operably coupled to receive the incoming clock signal, such that the second delay module generates a timing output signal, wherein the second delay module includes:

a second delay circuit operably coupled to the output port of the second flip flop such that the second delay circuit is capable of receiving the flip flop output signal and generating a second delay timing signal;

at least one clock speed adjusting circuit operably coupled to the second delay circuit;

a second multiplexer operably coupled to the at least one clock speed adjusting circuit and the delay circuit, wherein the second multiplexer has a select delay input port capable of receiving the select delay signal such that the second multiplexer generates a second multiplexer output signal corresponding to an output signal generated by at least one of: the at least one clock speed adjusting circuit and the delay timing signal; and

a third flip flop having an input port capable of receiving the second multiplexer output signal, an output port capable of providing the timing output signal and a timing port capable of receiving the incoming clock signal.

21. The apparatus of claim 20 further comprising:

a pseudo-random input generator operably coupled to the first flip flop, such that the pseudo-random input generator generates the input signal;

a sequencer operably coupled to the multiplexer, such that the sequencer generates the select delay signal;

a logic gate coupled to the second flip flop such that the logic gate receives the timing output signal and generates a timing indicator signal; and

a register coupled to receive the select delay signal and the timing indication signal.

22. The apparatus of claim 21 further comprising:

a plurality of control timing flip flops operably coupled to the pseudo random generator and coupled to receive the incoming clock signal such that the plurality of control timing flip flops generate a control timing signal, wherein the control timing signal is provided to the logic gate for comparison with the timing indicator signal; and

a logic gate flip flop coupled between the logic gate and the register wherein the logic gate flip flop is operably coupled to receive the incoming clock signal and the select delay signal and generate a timing result signal provided to the register.

23. A method of determining processing speeds for a plurality of integrated circuits and categorizing the integrated circuits based on the determined processing speeds, the method comprising:

(a) selecting one of the plurality integrated circuits;

(b) providing an incoming timing signal to a first flip flop, a first delay module and a second delay module;

(c) providing a delay select signal to a first delay module and a second delay module;

(d) retrieving a timing output signal from the second delay module;

(e) repeating steps (b) through (d) until the processing speed of the integrated circuit is determined; and

(f) recording the processing speed of the integrated circuit.

24. The method of claim 23 further comprising:

(g) repeating steps (a) through (f) for each of the plurality of integrated circuits.

25. The method of claim 24 further comprising:

(h) binning the plurality of integrated circuits based on the recorded processing speed of each of the integrated circuits.

26. The method of claim 23 wherein the plurality of integrated circuits are disposed on a central wafer such that the step (f) further includes:

(f1) etching a processing speed indicator on each of the integrated circuits.

27. The method of claim 26 further comprising:

(g) repeating steps (a) through (f) for each of the plurality of integrated circuits;

(h) removing each of the integrated circuits from the central wafer; and

(i) binning the plurality of integrated circuits based on the recorded processing speed of each of the integrated circuits.

28. The method of claim 23 wherein:

first delay module includes:

a first delay circuit operably coupled to an output port of the first flip flop such that the first delay circuit is capable of receiving a flip flop output signal and generating a first delay timing signal;

at least one clock speed adjusting circuit operably coupled to the first delay circuit;

a first multiplexer operably coupled to the at least one clock speed adjusting circuit and the delay circuit, wherein the first multiplexer has a select delay input port capable of receiving the select delay signal such that the first multiplexer generates a first multiplexer output signal corresponding to at least one of: an output signal generated by the at least one clock speed adjusting circuit and the delay timing signal; and

a second flip flop having an input port capable of receiving the first multiplexer output signal, an output port capable of providing the interim timing output signal and a timing port capable of receiving the incoming clock signal; and

the second delay module includes:

a second delay circuit operably coupled to the output port of the second flip flop such that the second delay circuit is capable of receiving the flip flop output signal and generating a second delay timing signal;

at least one clock speed adjusting circuit operably coupled to the second delay circuit;

a second multiplexer operably coupled to the at least one clock speed adjusting circuit and the delay circuit, wherein the second multiplexer has a select delay input port capable of receiving the select delay signal such that the second multiplexer generates a second multiplexer output signal corresponding to an output signal generated by at least one of: the at least one clock speed adjusting circuit and the delay timing signal; and

a third flip flop having an input port capable of receiving the second multiplexer output signal, an output port capable of providing the timing output signal and a timing port capable of receiving the incoming clock signal.